element of the claim. *See* MPEP 2131. The identical invention must be shown in as complete detail as is contained in the claim. *See id.* (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989). As regards Applicants' recited compiler, the Examiner cites Saleeba pg. 60, Section 2, first paragraph, and the portions of Saleeba that describe fig. 1. Respectfully, although a compiler is mentioned in these sections, these sections do not describe that this compiler can individually access or individually configure cells of the system. These sections apparently describe that the compiler can operate by splitting a program into parts that are to be executed directly in hardware and less critical parts to be executed in software, and that sections of an array can be reconfigured dynamically. However, these section do not describe that this compiler can individually access or individually configure cells of the system.

Claims 60 and 61 depend from claim 57. Thus, the arguments presented above in connection with claim 57 apply equally to claims 60 and 61.

For at least the above reasons, withdrawal of the rejection of claims 57 and 60-61 is respectfully requested.

II. REJECTION OF CLAIMS 62, 64, AND 68 UNDER 35 U.S.C. 103(a)

Claims 62, 64, and 68 stand rejected under 35 U.S.C. 103(a), the Examiner contending these claims are obvious in light of Saleeba. Claim 62 is directed to a data processor comprising cells and a compiler which receives state information regarding the state of a functional unit and transmits reconfiguration data to a cell as a function of the received state information.

To establish a prima facie case of obviousness, the prior art reference(s) must teach or suggest ALL the claim limitations. *See* MPEP 2143.

Applicant submits that there is absolutely no teaching

or suggestion in Saleeba of a compiler which receives state information regarding a first functional unit and transmits reconfiguration data to at least one of the cells as a function thereof. The Examiner points out that Saleeba mentions a state machine on page 64, first full paragraph, and argues it would have been obvious to utilize this state machine to inform the compiler of the state of configured functional units because the state machine would provide the necessary information for reconfiguration during runtime within Saleeba's system, which would improve the performance of Saleeba's system. Applicants respectfully submit that this is a completely hindsight reconstruction. Respectfully, Saleeba mentions use of a state machine to create a processor constructed from reconfigurable logic, but does not even suggest how such a state machine would be used. There is no suggestion of use of this state machine in connection with a functional unit, let alone, a compiler which receives information regarding the state of a functional unit and transmits reconfiguration data as a function thereof.

With respect to claims 64 and 68, these claims depend from claim 62; accordingly, the arguments presented above in connection with claim 62 apply equally to claims 64 and

In view of the foregoing, withdrawal of the rejection of claims 62, 64, and 68 is respectfully requested.

III. REJECTION OF CLAIMS 15-20, 29-31, 35-36, 38-48, 50-56, 79, AND 82-86 UNDER 35 U.S.C. 103(a)

Claims 15-20, 29-31, 35-36, 38-48, 50-56, 79, and 82-86 stand rejected under 35 U.S.C. 103(a), the Examiner contending that these claims are obvious over Schmidt (U.S. Patent 5,410,723) in view of Saleeba.

Applicant's claim 15 is generally directed to a parallel data processing apparatus that can be arithmetic-logically configured and reconfigured. The Examiner admits that the cited Schmidt reference does not teach or suggest "arithmetic-logically configuring the computing cell prior

to processing the input signals" and proposes a combination with Saleeba to remedy this deficiency.

Applicants respectfully submit that the proposed importation of Saleeba's dynamic reconfigurability is a purely hindsight reconstruction. The Examiner contends that this would improve Schmidt's system by optimizing computing cells more efficiently. The processor described by Schmidt is a wavefront processor and is, by its nature, not reconfigurable at run-time, and accordingly is restricted to operations that can be performed on a fixedly arranged array of processors, teaching away from the proposed combination. It is improper to combine reference where the references teach away from their combination. MPEP 2145.X.D.2 (citing *In re Grasselli*, 713 F.2d 731, 743).

Claim 16 depends from claim 15. Accordingly, the arguments presented above in connection with claim 15 apply equally to claim 16. Moreover, the Examiner admits that Schmidt combined with Saleeba does not teach the limitation recited by claim 16. The Examiner takes Official Notice that it would be obvious to use a multiplexer in the coupling unit in order to provide a switching device for the reconfiguring of the computing cells. The Applicant traverses the Official Notice and respectfully requests the Examiner cite a reference or provide an affidavit in support of the rejection. *See* MPEP 2144.03.

Claim 17-20, 79, 82, and 83 depend from claim 15. Accordingly, the arguments presented above in connection with claim 15 apply equally to claims 17-20, 79, 82 and 83. Moreover, as regards claim 18, the subject matter recited therein is generally directed to a system where <u>non-adjacent</u> cells may be coupled. Schmidt describes a wavefront processor that relies exclusively on <u>nearest neighbor</u> connections. Thus, the proposed combination neither teaches nor suggests Applicant's claim 18.

Claims 29-31 depend from claim 15. Accordingly, the arguments presented above in connection with claim 15 apply equally to claims 29-31. No reference is provided for the

specific features added by dependent claims 29-31, or for the motivation to combine the Schmidt and Saleeba references and/or other added features. To the extent the Examiner is taking official notice of either the limitations or the motivation to combine, Applicants traverse the Official Notice and respectfully requests the Examiner cite a reference or provide an affidavit in support of the rejection. See MPEP 2144.03.

Previously amended claim 35 is generally directed to a configurable and reconfigurable parallel processor with bus interconnections between the computing cells. The Examiner contends the combination of Schmidt and Saleeba render this claim obvious.

The Applicant respectfully traverses this rejection for reasons similar to those given for claim 15 above: there is no proper teaching to combine the references, and the references teach away from the proposed combination. Moreover, claim 35 recites buses which connect the computing cells. Although Schmidt describes buses in his wavefront processor, these buses are not for connecting computing cells, but rather for input and output from outside the processor. For this additional reason, the proposed combination is not the invention claimed in Applicant's claim 35. Withdrawal of the rejection of claim 35 is respectfully requested.

Claim 36 and 38-46 depend from claim 35; accordingly, the arguments presented above in connection with claim 35 apply equally to claims 36 and 38-46. Moreover, with respect to claims 39-41, the Examiner admits that neither Schmidt nor Saleeba disclose an external computer and memory device. However, the Examiner has not cited an additional reference for the specific limitations added by these claims. To the extent the Examiner is taking official notice of either the limitations or the motivation to combine, Applicants traverse the Official Notice and respectfully requests the Examiner cite a reference or

provide an affidavit in support of the rejection. *See* MPEP 2144.03.

Claim 47 recites buses interconnecting the plurality of logic elements. This feature is not found in the Schmidt reference, as discussed above for claim 35. Moreover claim 47 includes arithmetic-logical configurability features previously discussed above for claim 15. These features are not taught or suggested by the combination of Schmidt and Saleeba.

Claims 48, 50-56, 84, and 85 depend from claim 47. Thus, arguments presented above in connection with claim 47 apply equally to claims 48, 50-56, 84 and 85. Moreover, the additional subject matter recited in, for example, claims 50 and 51 are found in neither Schmidt nor Saleeba, e.g., the peripheral interface. To the extent the Examiner is taking official notice of either the limitations or the motivation to combine, Applicants traverse the Official Notice and respectfully requests the Examiner cite a reference or provide an affidavit in support of the rejection. *See* MPEP 2144.03.

With respect to claim 86, the Examiner has relied on the combination with Saleeba to provide a reconfiguration capability to the Schmidt reference. As discussed above with respect to claim 15, Applicants respectfully submit that this combination is not proper, and, in fact, the references teach away from the proposed combination.

For at least the foregoing reasons, the rejection of claims 15-20, 29-31, 35-36, 38-48, 50-56, 79, and 82-86 should be withdrawn.

IV. REJECTION OF CLAIM 58 OVER SALEEBA IN LIGHT OF SCHMIDT

Claim 58 stands rejected under 35 U.S.C. 103(a), the Examiner contending it is obvious over Saleeba in view of Schmidt. Claim 58 depends from claim 57. Thus, the arguments presented above in connection with claim 58 apply equally to claim 57.

Moreover, Applicants respectfully submit that neither Schmidt nor Saleeba teaches or suggests the use of state information from a cell by a compiler. Simply having what the Examiner terms state information for the cells in Schmidt, does not teach or suggest the use of this information by a compiler. There is also no teaching or suggestion of regrouping cells based on received state information. To establish a prima facie case of obviousness, the prior art reference(s) must teach or suggest ALL the claim limitations. *See* MPEP 2143. Accordingly, the proposed combination can not be used to make out a prima facie case of obviousness for Applicant's claim 58.

Withdrawal of the rejection of claim 58 is thus respectfully requested.

CONCLUSION

In view of all of the above, it is believed that all issues raised by the Examiner have been added. It is respectfully submitted that all pending claims are in condition for allowance. Passage to issuance is, therefore, requested.

Respectfully submitted,

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By: _____

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